CLAIMS:

1. An integrated circuit, comprising:

a plurality of inputs;

a plurality of outputs; and

a test arrangement being coupled between the plurality of inputs and the plurality of outputs in a test mode of the integrated circuit, the test arrangement comprising a plurality of logic gates, each logic gate from the plurality of logic gates having a first input coupled to an input from the plurality of inputs;

characterized by each logic gate from the plurality of gates having a further input coupled to a fixed logic value source.

2. An integrated circuit as claimed in claim 1, characterized by further comprising a functional block being coupled between the plurality of inputs and the plurality of outputs in a functional mode of the integrated circuit.

3. An integrated circuit as claimed in claim 1, characterized in that the plurality of logic gates comprises exclusive logic gates.

4. An integrated circuit as claimed in claim 1 or 3, characterized in that the fixed logic value source is programmable.

5. An integrated circuit as claimed in claim 1 or 3, characterized by further comprising a plurality of multiplexers, a multiplexer from the plurality of multiplexers being responsive to a select signal, the multiplexer having a first input coupled to an input from the plurality of inputs, a second input coupled to the fixed logic value source of a logic gate from the plurality of logic gates and an output coupled to the further input of the logic gate.

6. An integrated circuit as claimed in claim 5, characterized in that the select signal is provided by the test arrangement.

7. An integrated circuit as claimed in claim 5, characterized in that the select signal is provided via a dedicated input from the plurality of inputs.